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## (54) Digital-to-analogue conversion.

(57) The converter incorporates a transversal filter. The filter delays are implemented in digital form prior to conversion into analogue signals (preferably using switched capacitor techniques). One form of switched capacitor converter (with or without filtering) employs a single capacitor, common to a plurality of bits, appropriate weighting of the bits being achieved by controlling the switching.

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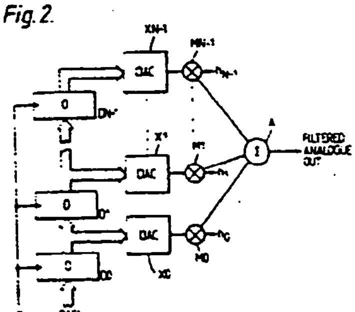
Fig. 2.



# DIGITAL-TO-ANALOGUE CONVERSION

The present invention relates to digital-to-analogue converters and digital-to-analogue converters incorporating a filtering function and is particularly (though not exclusively) concerned with their implementation using switched-capacitor techniques.

A typical, conventional arrangement is shown in Figure 1, where successive sample values of a w-bit digital word $[b_o b_1 ... b_i ... b_{w-1}]$ are supplied to a digital-to-analogue converter (DAC) 1 followed by an analogue FIR (finite impulse response) filter 2, based on a conventional tapped delay line structure with delays $z^{-1}$, filter coefficient multipliers $h_o ... h_{N-1}$ and an adder (or of course a parallel structure may be used). The coefficients are selected to give any desired filter response; in general this will be a baseband response from DC to half the sampling frequency $F_s$, followed by some rejection of unwanted frequencies above $F_s/2$.

The DAC may employ switched capacitor techniques (as described for example in Roubik Gregorian - "High Resolution Switched Capacitor D/A Converter" -Microelectronics Journal, Vol. 12, No. 2, 1981 Mackintosh Publ. Ltd.); in the filter, the analogue delays may also be realised by switched-capacitor elements. The realisation of the analogue delays may however not be ideal.

According to one aspect of the present invention there is provided an apparatus for producing a filtered analogue output signal from a digital input signal, comprising
- digital-to-analogue conversion means;
- delay means for producing a plurality of mutually delayed signals;
- means for forming the sum of the mutually delayed signals, weighted by factors corresponding to a desired filter response;

characterised in that
- the delay means precedes the digital to analogue conversion means and the digital to analogue conversion means is arranged to convert each of the mutually delayed digital signals into analogue form.

In another aspect, the invention provides a switched-capacitor digital-to-analogue converter comprising inputs for receiving signals representing respective bits of a digital signal, respective switching means for supplying charge to capacitance in dependence of the states of those bits, and means for generating an analogue output signal representing the sum of these charges, characterised in that the said capacitance is a single capacitance common to all the bits and that the switching means are arranged to supply charge to the capacitor for respective different total switching times such that the charges supplied are weighted acording to the significance of the bits.

Some embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

- Figure 2 is a block diagram of one form of filtered digital-to-analogue converter according to the invention;
- Figure 3 is a circuit diagram of a known switched-capacitor unit which may be employed in the converter of Figure 1;
- Figure 3a illustrates clock pulses used by the unit of Figure 3;
- Figure 4 is a block diagram of a further embodiment of filtered digital-to-analogue converter;
- Figure 5 is a modified version of part of Figure 3, for implementing negative filter coefficients;
- Figure 6 is a circuit diagram of a digital-to-analogue converter unit according to a further embodiment of the invention;
- Figure 7 illustrates the clock and switching pulses employed in the unit of Figure 6;

Figure 8 is a block diagram of a filtered digital-to-analogue converter employing converter units of the type shown in Figure 6;

- Figure 9 is a modified version of part of Figure 6, for implementing negative filter coefficients;
- Figure 10 illustrates a practical implementation of the converter of Figure 8;

Figure 11 is a block diagram of a pulse generator for driving the converter of Figure 10; and

- Figure 12 is a state diagram illustrating the operation of the generator of Figure 10.

The filtered digital-to-analogue conversion apparatus shown in Figure 2 receives, as does that of Figure 1, successive w-bit digital samples of a signal to be converted. The digital words are fed to a chain of N w-bit wide D-type bistable flip-flops DO...DN-1 which are clocked at sampling rate $F_s$ with clock pulses $\phi$, so that a digital word, delayed by a respective number of sample periods, is available at the output of each flip-flop. These outputs are converted into analogue form by digital-to-analogue converters X0... XW-1 which produce at their outputs successive analogue samples corresponding to the digital samples supplied to them. The analogue outputs are multiplied by respective filter coefficients $h_o ... h_{N-1}$; multipliers M0...MN-I are

shown though in practice it may be more convenient to achieve the same effect by applying appropriate reference voltages to the converters X0 etc. The weighted analogue values are then summed in an adder A.

It will be seen that the arrangement of Figure 2 performs the same conversion and filtering function of the Figure 1 arrangement, but realises the necessary delays digitally in a simple manner, at the expense however of increasing the number of digital-to-analogue converters to N (the length of the desired filter impulse response).

In principle, any suitable digital-to-analogue converters may be used for the converters XO ... XN-I, but preferably switched capacitor converters such as the (known) converter shown in Figure 3 may be employed.

In Figure 3, the input bits of a w-bit digital word are designated $b_o...b_{w-1}$ and each serves to switch, according to its binary value, an electronic switch CS0...CSw-I (shown schematically) between zero volts (referred to below as "ground") and a reference voltage $V_R$. The converter contains a number of electronic switches controlled by the non-overlapping two-phase clock pulses $\phi_0$, $\phi_1$ at the sampling frequency $F_s$, which are shown in Figure 3a. In Figure 3 and elsewhere, the switches are shown as rectangles containing 0 or 1 indicating that the switch is closed during clock phase 0 or 1 respectively. Using the suffix i to indicate generically the components handling signals from one bit ($b_i$) of the input bits $b_o...b_{w-1}$, the output of each switch CSi is connected via a switch S1i controlled by $\phi_1$ to one side of a capacitor CPi, which is also connected to ground via a switch S0i controlled by $\phi_o$. The other side of each capacitor CPi is connected to a common node ND, also connected to ground by a switch S1 controlled by $\phi_1$. The capacitors have binary weighted values - ie the capacitance of the capacitor CPi is $2^i$.C where C is the value of the smallest capacitor CPO. The node ND is also connected via a switch S0 controlled by $\phi_o$ to the input of a high gain inverting amplifier OA which has a negative feedback path consisting of a capacitor $C_F$ in parallel with a switch S1F controlled by $\phi_1$.

During clock phase 1, the capacitor $C_F$ is discharged via S1F. Also, each capacitor CPi is charged or discharged via switches S1i and S1 to the voltage (0 or $V_R$) determined by the respective switch CSi. During clock phase $\phi_o$, the total charge on the capacitors CPi

$$Q = \sum_{0}^{w-1} b_i . V_R . 2^i . C = CV_R \sum_{0}^{w-1} b_i 2^i$$

is transferred to the capacitor $C_F$ so that the output of the converter is

$$V_O = \frac{C}{C_F} V_R \sum_{i=0}^{w-1} b_i 2^i \qquad ...(1)$$

Although converters of the design shown in Figure 3 could be used directly to replace the converters XO...XN-I of Figure 2, a more practical arrangement is shown in Figure 4 where the node ND, switches S0, S1, SIF, capacitor $C_F$ and amplifier OA are common to the N converters. The flip-flops are as in Figure 2, whilst the capacitor/switch array units CSA0...CSAN-I correspond to the components enclosed in the broken line box in Figure 3. In this embodiment, the capacitor values in each array are chosen to weight the contribution of that array to the final output by a factor corresponding to the appropriate one of the desired filter coefficients $h_o...h_{N-I}$.

To accommodate negative coefficients, the array is modified by the transposition of the clock pulses illustrated in Figure 5 by transposition of switches S0i and Sli. The nth array (n=0,....,N-1) has capacitors with values $2^i.C_n$ where $C_n = |h_n|.C^*$ ($C^*$ being a constant), so that the contribution of this array to the total output voltage is

$$V_{o,n}(z) = \frac{h_n}{C_F} C^* V_R \left( \sum_{i=0}^{W-1} b_{i,n} . 2^i \right) . z^{-n} \qquad \ldots(2)$$

where z is the z-transform variable and $b_{i,n}$ is the value of the ith bit of the digital word at the output of the nth D-type flip-flop. The contribution of all N words for an FIR filter of length N is

$$V_o^{\cdot}(z) = \sum_{n=0}^{N-1} V_{o,n}(z)$$

$$V_o(z) = \frac{V_R}{C_F} . \sum_{n=0}^{N-1} \left[ h_n . C^* \left( \sum_{i=0}^{W-1} b_{i,n} . 2^i \right) . z^{-n} \right]$$

If we set $C_F = 2^W . C^*$ then the output voltage is

$$V_o(z) = V_R \sum_{n=0}^{N-1} h_n . \left( \sum_{i=0}^{W-1} b_{i,n} . 2^{i-W} \right) . z^{-n}$$

If the smallest capacitance value $C_n$ is C, and the corresponding value of $h_n$ is $h_{n\ min}$ then the remaining capacitor values are given by

$$C_n = \frac{|h_n|}{|h_n|_{min}} . C$$

and $$C_F = \frac{2^W . C}{|h_n|_{min}}$$

Since $C_F$ is usually the largest capacitor in the circuit, we obtain a maximum capacitance spread of

$$\frac{C_F}{C_{n\ min}} = \frac{2^W}{|h_{n\ min}|}$$

and a total capacitor area of

$$C_{total} = \frac{C}{|h_n|_{min}} \left[2^W + (2^W - 1) . \sum_{n=0}^{N-1} |h_n|\right]$$

For an example of FIR filtering function with equal coefficients and unity DC gain ($h_n = l/N$, $n = 0, ..., N-1$) the above results lead to a capacitance spread of $C_{spread} = N.2^w$ and a total capacitor area of $C_{total} = N.(2^{w+1}-1).C$.

The embodiment of Figure 4 requires (N.w + 1) capacitors and (2N.w + 3) switches, increasing with both the bit resolution w of the conversion and the length N of the desired filter impulse response. This means that, even for a medium bit resolution and short filter responses, the resulting silicon area required for an integrated circuit implementation can become rather large. An alternative converter is however now proposed, having reduced number of capacitors and switches.

Figure 6 shows a switched capacitor digital-to-analogue converter (without filtering). It can be employed alone, or, as will be described in more detail below, can be used to replace the converters X0...XN-1 of Figure 2, in the same manner as was the converter of Figure 3.

Input bits $b_i$ and switches CSi perform the same functions as in Figure 3, as do switches S1, S0, SF, capacitor $C_F$ and amplifier OA. However, the capacitors CPi and switches $S0_i$ are replaced by a single capacitor CP and switch S0A. The binary weighting of contribution of the w input bits is instead determined by the waveforms applied to the switches S1i (now designated SA0....SAi...SAw-1). Effectively the capacitor CP is multiplexed between the input bits. A set of switching waveforms $\phi'_1$, $\phi'_o$ and $A_o..A_{w-l}$ for $w = 3$ is illustrated in Figure 7.

Note that there are now $2^{w-1}$ clock pulses $\phi'_1$ (or $\phi'_o$ ) in one conversion period. The waveforms $A_0$ ...$A_{w-l}$ contain 1, 2, 4 etc pulses synchronous with $\phi_1$ - ie in general the waveform $A_i$ contains $2^i$ pulses. At the beginning of each conversion period, the feedback capacitor $C_F$ is reset by the switch SF controlled by pulse $A_o$. Pulse $A_o$ also closes switch $A_o$ and the capacitor CP assumes a voltage of 0 or $V_R$ according to the state of bit $b_o$. On the following clock pulse $\phi'_o$ this charge is transferred to $C_F$. This process is repeated by pulse $A_1$ for bit $b_1$; however, this occurs twice, as $A_1$ contains two pulses, and so forth, the D/A conversion being performed sequentially from bit $b_o$ to bit $b_{w-l}$. The converted output is available during pulse $\phi'_o$ following the last pulse of $A_{w-l}$, prior to resetting of $C_F$ by a further pulse $A_o$. Of course it is not actually necessary that the bits be processed in any particular sequence, or indeed that all the pulses for one particular bit be generated before those of another bit (though obviously the pulses must not coincide).

The equivalent bit voltage $V_i$ corresponding to each bit of the digital word is determined by the number of pulses of the corresponding switching waveform $A_i$ and can thus be expressed by

$V_i = V_R.b_i.2^i$

and therefore the converted output is

$$V_o = \frac{C}{C_F} V_R \sum_{i=0}^{w-1} b_i . 2^i$$

Assuming $[V_0 \max / V_R.(l-2^{-N})] = 1$, we can easily see from the above expression that the capacitance spread of the converter in Figure 6 is equal to the capacitance spread of the conventional converter of Figure 3, ie $(C_F/C) = 2^w$. However, the total capacitor area is now only $(2^w + 1).C$, compared to $2^{w+1}.C$ in a conventional converter, and the total number of capacitors has also been reduced from (w + 1) to only 2. An additional significant advantage of this new architecture is that, unlike conventional converters, the accuracy of the capacitance ratio $C_F/C$ does not affect the required bit resolution, which depends solely on the number of time slots of each switching waveform. Thus, we can easily apply to the converter of Figure 6 a number of well known design techniques than can significantly reduce the capacitance spread in a switched-capacitor network (eg capacitive-T network), even though this also bring an inherent reduction of the resulting accuracy of the capacitance ratios. This makes it practical to implement high resolution converters using simple switched capacitor networks occupying a small area of silicon.

It is observed that, for a given maximum switching frequency, the conversion rate (and hence sampling rate of the digital words that can be accomodated) is reduced by a factor of $(2^w-l)$ relative to Figure 3;

however the reduction in capacitor area and required capacitance ratio accuracy make this embodiment particularly useful for high resolution conversions at lower frequency.

An implementation of a combined digital-to-analogue converter and FIR filter based on the binary-weighted time slot array architecture described above is illustrated in Figure 8. The flip-flops Dn are shown as for Figures 2 and 4. The converters Xn of Figure 2 are replaced by time slot arrays TA0 to TAN-l, followed by common components S1, S0, OA, $C_F$ and SF which are identical to those shown in Figure 7. Each time slot array TAi is either in the form indicated in the dotted rectangle in Figure 7 (for positive $h_n$) or, for negative $h_n$ is structurally the same but is supplied with different pulses. Thus switches SAn supplied by pulses $A_n$ and switch SOA supplied with pulses $\phi_0'$ are replaced by switches SBn and S1A supplied with pulses $B_n$ and $\phi_1'$, as shown in Figure 9. Pulses $B_n$ (n=0...n-l) take the same form as pulses $A_n$ but are synchronous with $\phi_0'$ instead of $\phi_1'$.

As in the case of the architecture of Figure 2, we can easily see that the normalised output voltage conversion level corresponding to all N digital words is also expressed by

$$\frac{V_o(z)}{V_R(1-2^{-N})} = \frac{1}{C_F} \sum_{n=0}^{N-1} [C_n . ( \sum_{i=0}^{W-1} b_{i,n} 2^i ) . z^{-n}]$$

where $$C_n = \frac{|h_n| . C_F}{2^W}$$

in order to preserve the gain constant of the FIR transfer function. After normalisation, we obtain

$$C_{n\,min} = C$$

$$C_n = \frac{|h_n|}{|h_{n\,min}|} . C$$

$$C_F = \frac{2^W}{|h_{n\,min}|} . C$$

yielding a maximum capacitance spread of

$$C_{spread} = {}^{CF}/C = \frac{2^W}{|h_{n\,min}|}$$

and

$$C_{total} = \frac{C}{\left| h_{n\,min} \right|} \left( 2^{W} + \sum_{n=0}^{N-1} h_n \right)$$

for the total capacitor area. For many practical situations where the FIR filter is designed such that

$$\sum_{n=0}^{N-1} h_n = 1$$

the above expression for $C_{total}$ shows a reduction of about 50% over the total capacitor area obtained with the previous realisation. Two additional advantages of the architecture with binary-weighted time slot arrays are obtained firstly with respect to the total number of capacitors, which has been reduced from (N.w+1) to only (N+1), and, secondly, with respect to the required capacitance ratio accuracy of the impulse response coefficients of the FIR filter.

Figures 10 and 11 illustrage a simple practical implementation of the type of combined digital-to-analogue converter decribed above with reference to figure 8. It has 4-bit resolution and four equal FIR filter coefficients. The filter impulse response (in z-transform notation) is

$H(z) = \frac{1}{4}(1 + z^{-1} + z^{-2} + z^{-3})$.

There are four 4-bit wide D-type flip-flops D0, DI, D2, D3. Note that the fist of these is (as in the other figures) not strictly necessary but is included to ensure accurate timing. Also the switches CSi are omitted (on the basis that, for a 4-bit implementation, the voltages output directly from the flip-flops are themselves sufficiently consistent). There are three stages TAN0 ... TAN3, of the type shown in figure 6, with equal capacitor C0 ... C3 (= capacitance C) representing the four equal coefficients. Components S0, S1, SF, CF and OA are as shown in figure 6, whilst two simple sample and hold circuits SHI, CH1, OA1, SH2, CH2, OA2 are included to sample the output ($A_0$ being applied to switches SH1, SH2) when conversion is completed, to eliminate any output transients during conversion. $C_F$ is equal to 64C for Vomax/$V_R$ $(1 - 2^{-N})$ = 1.

The switching waveforms $A_0$, $A_1$, $A_2$, $A_3$ are generated by means of the generator shown in figure 11. A square-wave oscillator OSC drives a non-overlapping phasing generator consisting of an invertor I1, cross-coupled NAND gates N1, N2, and inverters I2, I3 to produce pulses $\phi_0'$ , $\phi_1'$ . A modulo 8 binary down-counter Z1 is clocked by $\phi_1'$ . The '1111' state is designated as an idle-state in which the counter is locked by an and-gate AND1 which decodes this state to an end of conversion pulse EOC and inhibits clock pulses via a switch SWI in the oscillation circuit.

The generation of the required $(2^{w}-1) = 15$ pulses of the switching waveforms $A_0$ ... $A_3$ is indicated by an external pulse SOC (synchronous with the digital input data to be converted) which is applied to a paralled load input PE of the counter Z1 to load count '1110' into the counter.

The counter is then decremented by pulses $\phi_1'$ through its states to 000, during which period the counter states are decoded by inverters I4 ... I7 and and-gates AND1 ... AND4 to produce the pulses $A_0$ ... $A_3$ as illustrated in the sequence diagram in figure 12. The sixteenth pulse $\phi_1'$ returns the counter to the '1111' state where it remains locked until a further start pulse SOC is received.

Note that in this converter, pulses $B_i$ are not required (since the filter coefficients are all positive) but could of cause be generated by a second counter and decoding logic similar to the arrangements for $A_i$.

A discrete component version of this converter can be constructed using amplifiers type LF353, CMOS analogue switches type CD4016, and standard CMOS logic circuits, although in practice an integrated circuit implementation is to be preferred.

Typical capacitor values are C = 40pF and $C_F$ = 2700pF (with ± 0.2% of the nominal values) may be used.

## Claims

1. An apparatus for producing a filtered analogue output signal from a digital input signal, comprising
- digital-to-analogue conversion means;
- delay means for producing a plurality of mutually delayed signals; and
- means for forming the sum of the mutually delayed signals, weighted by factors corresponding to a desired filter response;

characterised in that the delay means precedes the digital to analogue conversion means and the digital to analogue conversion means is arranged to convert each of the mutually delayed digital signals into analogue form.

2. An apparatus according to claim 1, characterised in that the digital-to-analogue conversion means employs switched capacitors.

3. An apparatus according to claim 2, characterised in that the digital-to-analogue conversion means comprises, for each of the said mutually delayed digital signals, respective switched capacitor means for forming a charge dependent on the value represented by the relevant digital signal, and common means for forming an analogue output signal representing the sum of the charges.

4. An apparatus according to claim 3, characterised in that at least one of the switched capacitor means contains a capacitor or capacitors which differ(s) in value from the corresponding capacitor or capacitors in another of the switched capacitor means, such as to weight the charges by factors corresponding to the desired filter response.

5. An apparatus according to claim 2, 3 or 4, characterised in that the digital-to-analogue conversion means comprises, for each of said mutually delayed digital signals, respective switched capacitor means each comprising switching means for supplying, in dependence on the state of bits of the relevant digital signal, charge to a single capacitance which is common to all the bits of that signal, and that the switching means are arranged to supply charge to the capacitor for respective different total switching times such that the changes supplied are weighted according to the significance of the bits.

6. An apparatus for producing a filtered analogue output signal from a digital input signal, substantially as herein described with reference to the accompanying drawings.

7. A switched-capacitor digital-to-analogue converter comprising inputs for receiving signals representing respective bits of a digital signal, respective switching means for supplying charge to a capacitance in dependence of the states of those bits, and means for generating an analogue output signal representing the sum of those charges, characterised in that the said capacitance is a single capacitance common to all the bits and that the switching means are arranged to supply charge to the capacitor for respective different total switching times such that the charges supplied are weighted according to the significance of the bits.

8. A switched-capacitor digital-to-analogue converter substantially as herein described with reference to the accompanying drawings.

Fig.1.
PRIOR ART

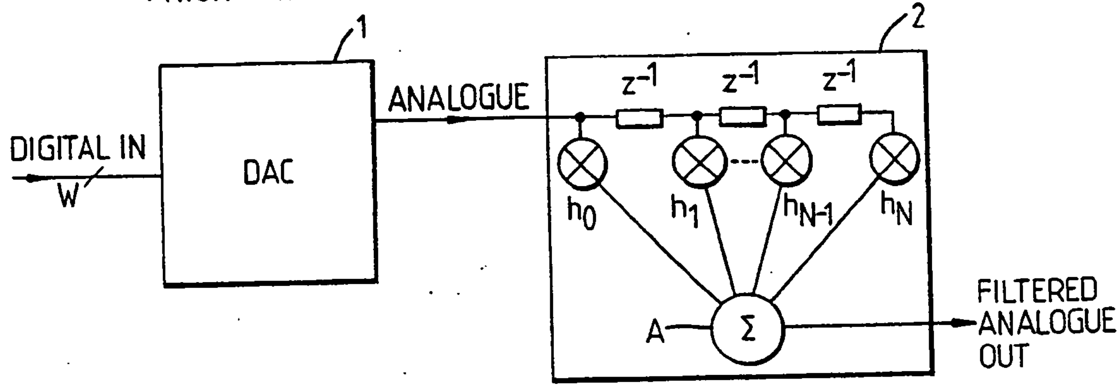
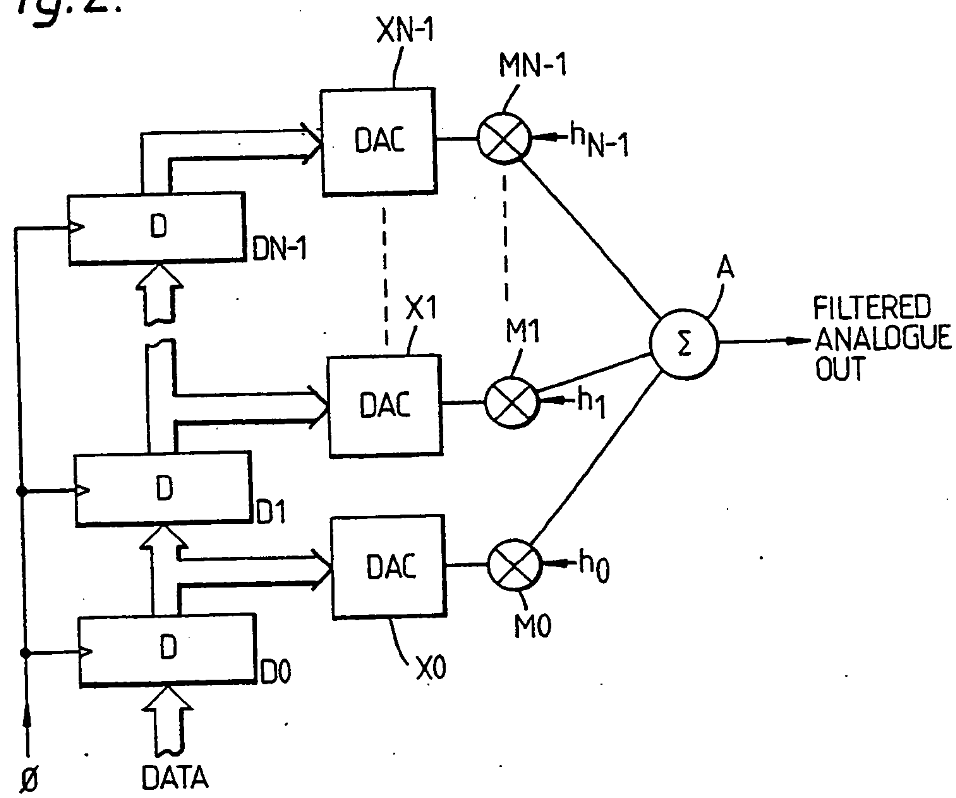



Fig.2.



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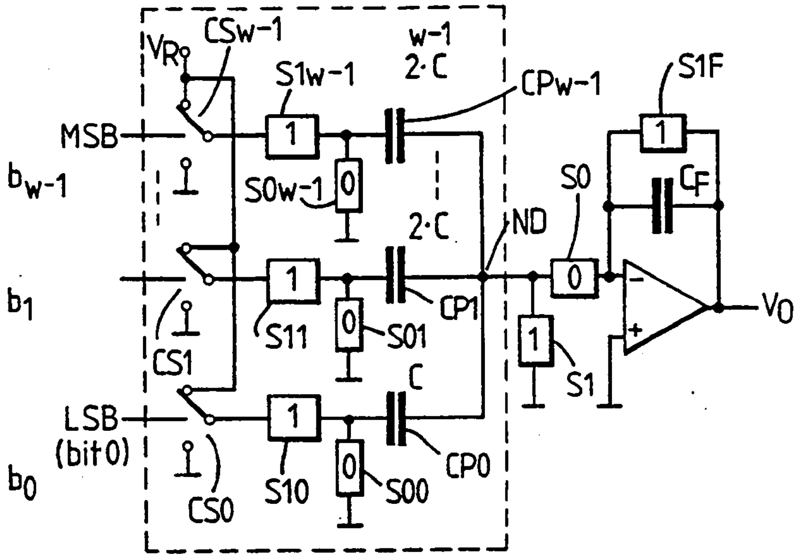



Fig. 3.
(PRIOR ART)

Fig. 3a

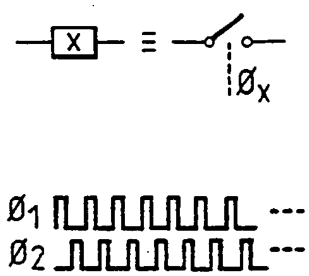



Fig. 4.

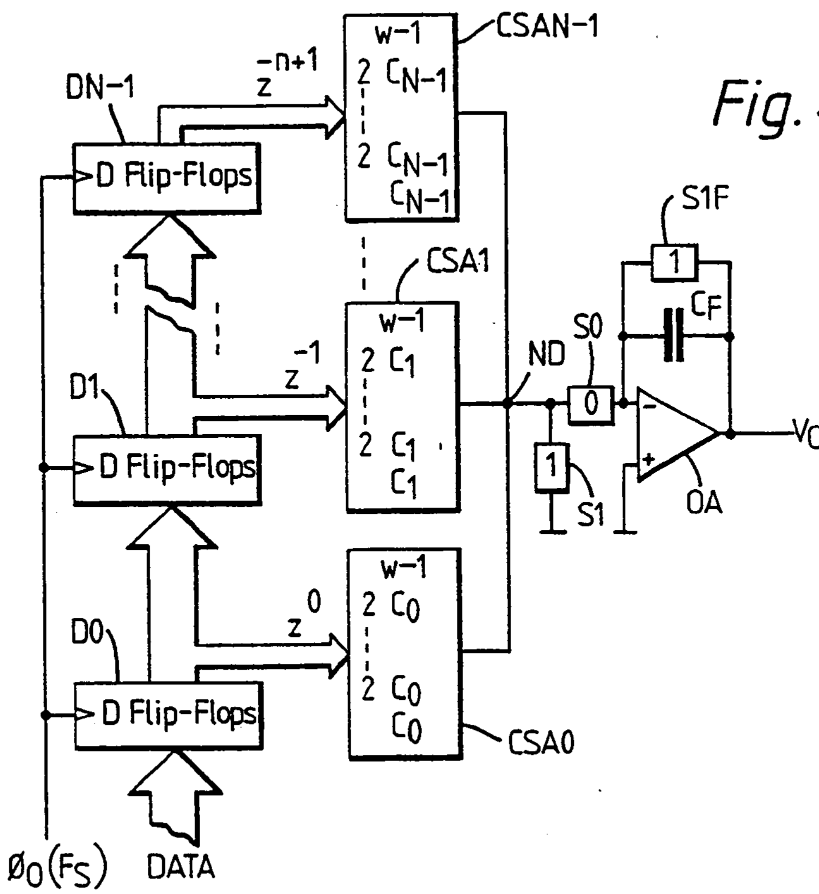
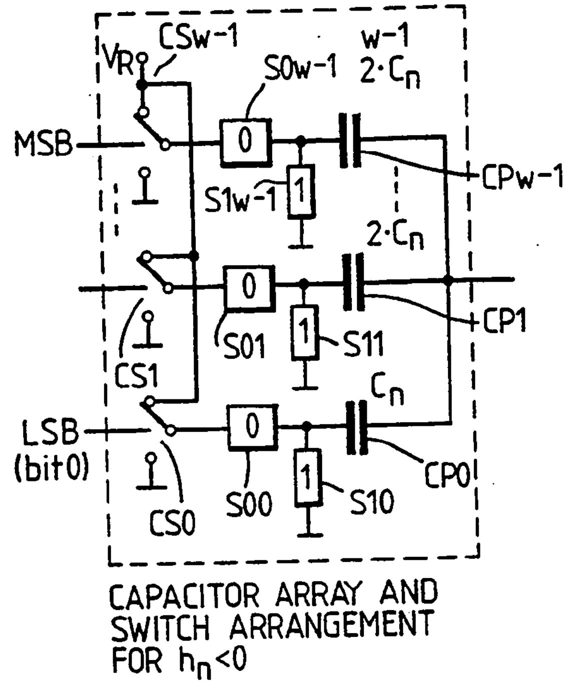


Fig.5.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S0w-1
w-1
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MSB
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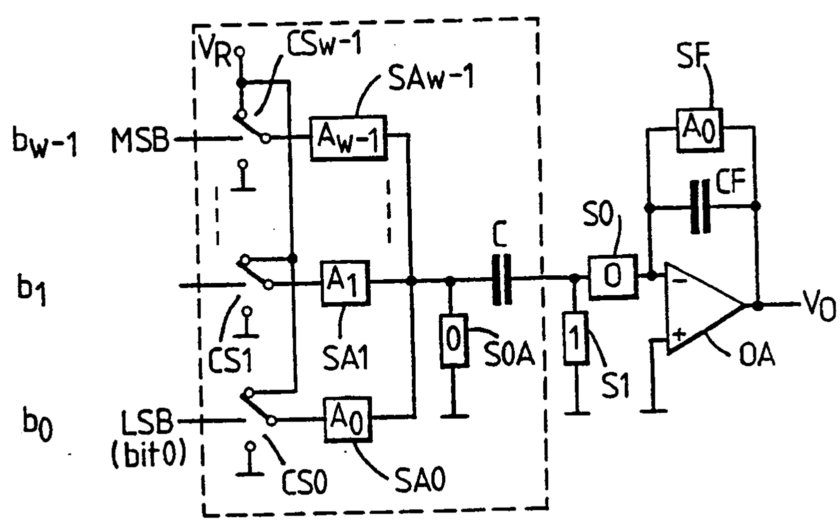
S1w-1
1
CPw-1
2·Cn
0
CP1
CS1
S01
1
S11
Cn
LSB
(bit0)
0
CP0
CS0
S00
1
S10
CAPACITOR ARRAY AND SWITCH ARRANGEMENT FOR hn<0

Fig.6.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CF
C
S0
b1
A1
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SA1
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S0A
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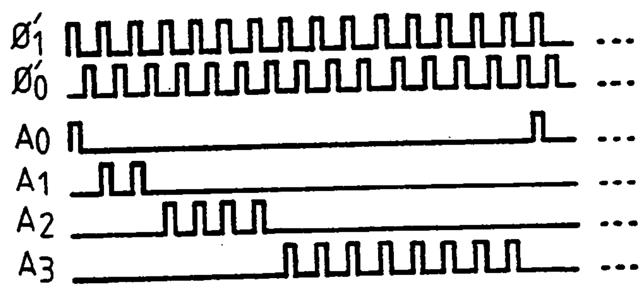
S1
OA
b0
LSB
(bit0)
A0
CS0
SA0

Fig. 7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A0
A1
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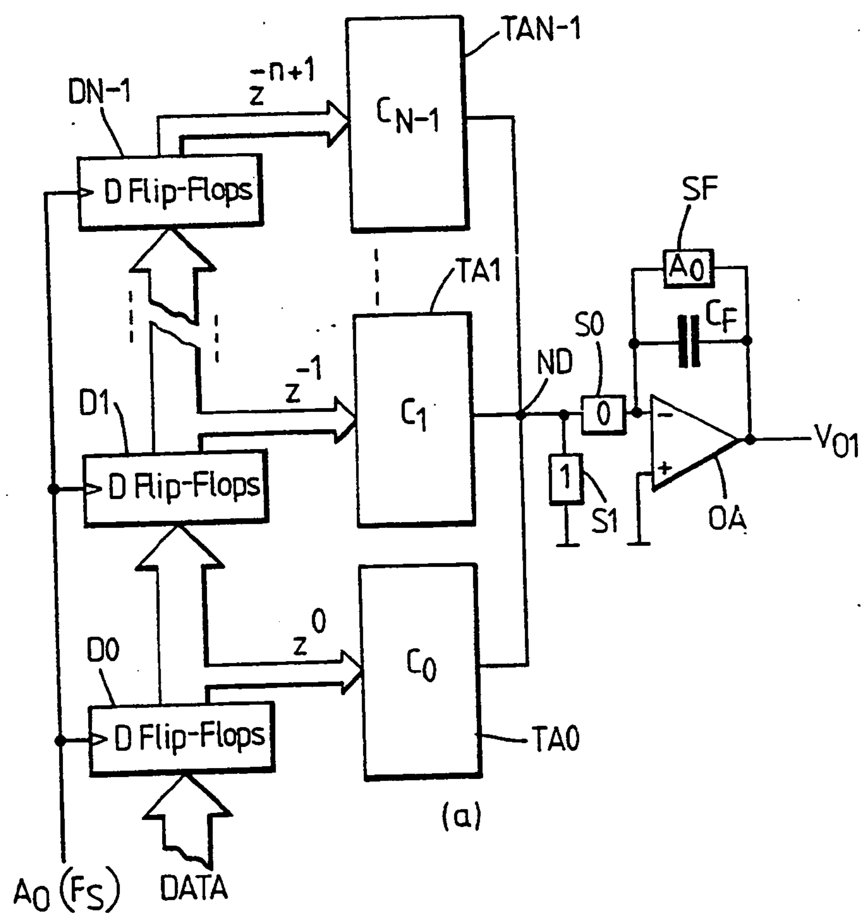
A3

Fig. 8.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TA1
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D1
$C_1$
0
$V_{01}$
D Flip-Flops
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S1
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$C_0$
D Flip-Flops
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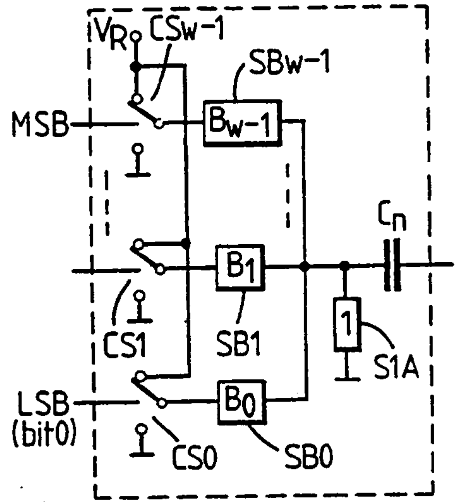
(a)
A0 (FS)
DATA

Fig. 9.



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MSB
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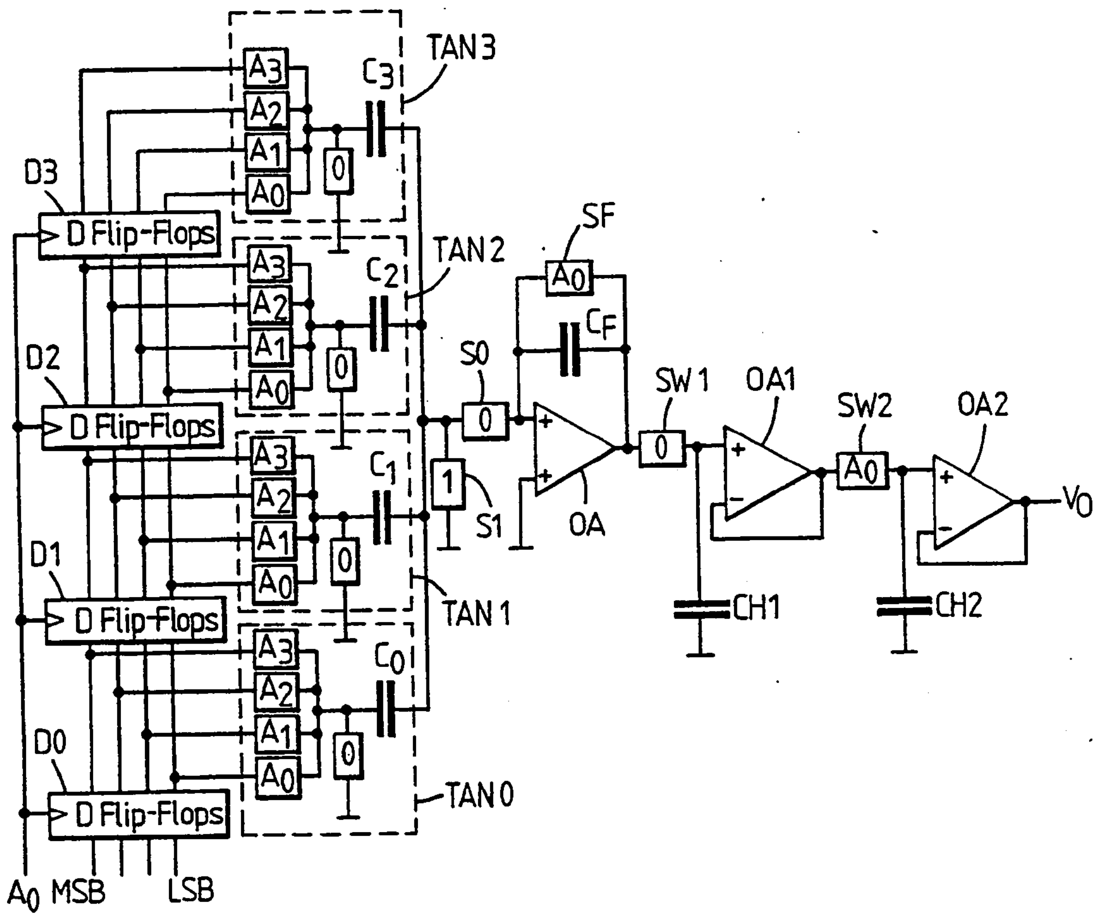
Fig.10.



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D2
D Flip-Flops
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S1
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SW2
OA2
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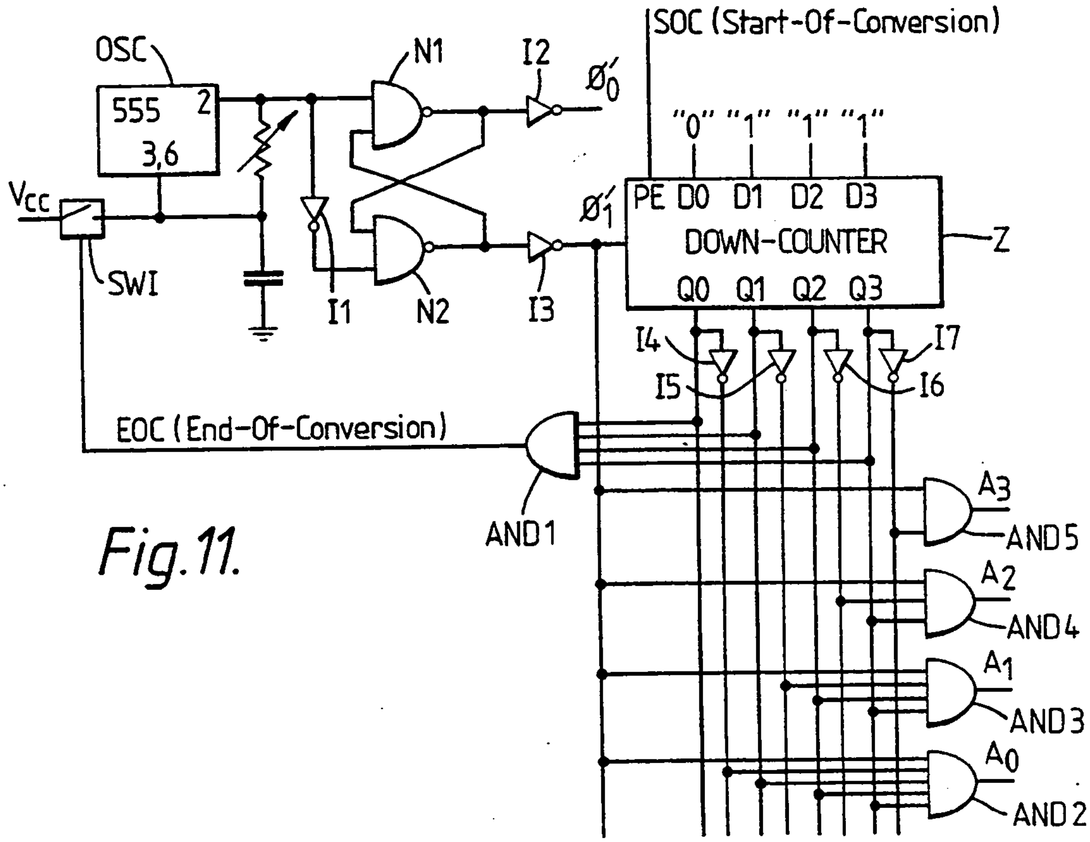
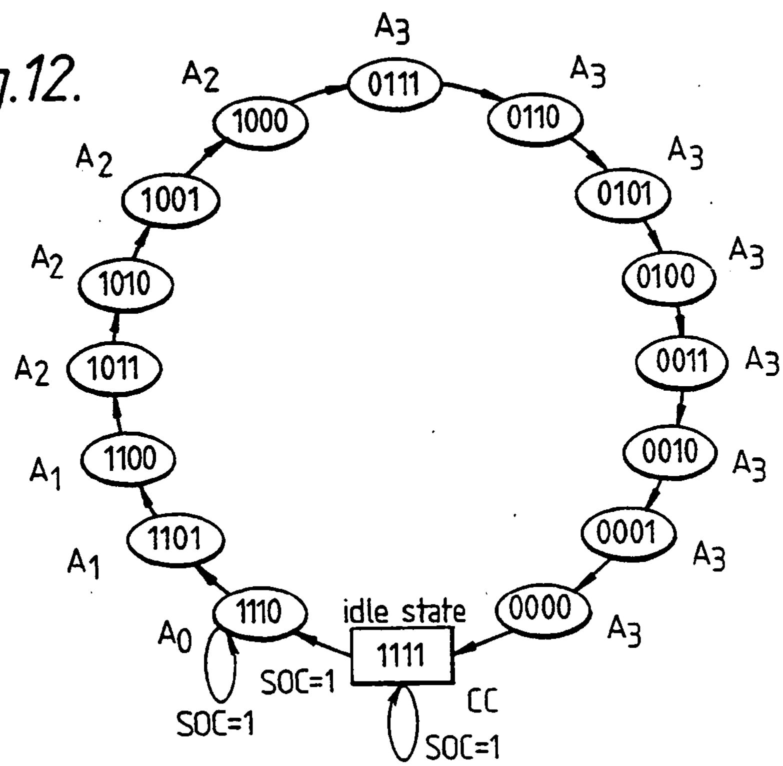
D Flip-Flops
TAN 1
CH1
CH2
C0
D0
TAN0
D Flip-Flops
A0
MSB
LSB



SOC (Start-Of-Conversion)
OSC
555
2
3,6
N1
I2
Ø'0
"0" "1" "1" "1"
Vcc
SWI
I1
N2
I3
Ø'1
PE D0 D1 D2 D3
DOWN-COUNTER
Z
Q0 Q1 Q2 Q3
I4
I5
I6
I7
EOC (End-Of-Conversion)
AND1
A3
AND5
A2
AND4
A1
AND3
A0
AND2


Fig.11.

Fig.12.



A3
0111
A2
1000
A3
0110
A2
1001
A3
0101
A2
1010
0100
A3
A2
1011
0011
A3
A1
1100
0010
A3
A1
1101
0001
A3
1110
idle state
0000
A0
1111
A3
SOC=1
CC
SOC=1
SOC=1

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 89 30 5396

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.4) |
|---|---|---|---|
| A | GB-A-2 171 568 (PLESSEY)<br>* Page 3, lines 22-35; figure 9 * | 1 | H 03 H 17/02<br>G 06 J 1/00<br>H 03 M 1/66 |
| A | ELEKTOR, vol. 9, no. 1, January 1983, pages 1.36-1.42, Canterbury, Kent, GB; "Chips for digital audio"<br>* Figure 6 * | 1 | |
| A | IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-18, no. 6, December 1983, pages 745-753, IEEE, New York, US; A.M. CHIANG et al.: "A high-speed digitally programmable CCD transversal filter"<br>* Page 749, paragraph III - page 750, column 1, last line; figure 6 * | 1 | |
| A | US-A-4 620 158 (YASUKAWA)<br>* Whole document * | 1 | |
| A | US-A-4 616 212 (LAW)<br>* Abstract; figure * | 2,3 | TECHNICAL FIELDS SEARCHED (Int. Cl.4)<br>H 03 H<br>G 06 J<br>H 03 M |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 24-08-1989 | GUIVOL Y. |

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